

CYCLE	OPERATION	BANK
0	READ	0
1	WRITE	1
2	READ	2
3	WRITE	3
4	PAUSE	
5	WRITE	0
6	READ	1
7	WRITE	2
8	READ	3
9	PAUSE	

FIG.I

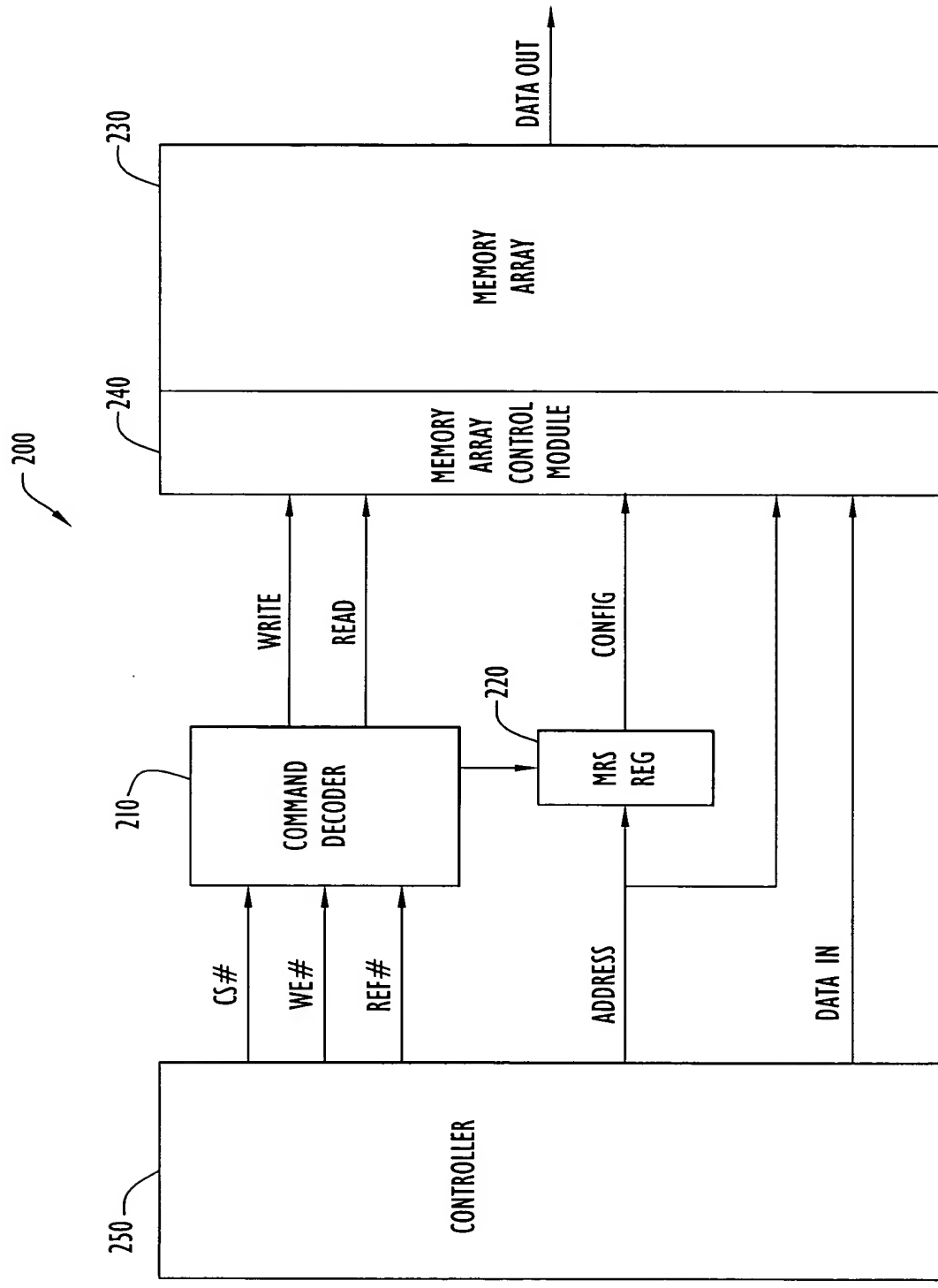
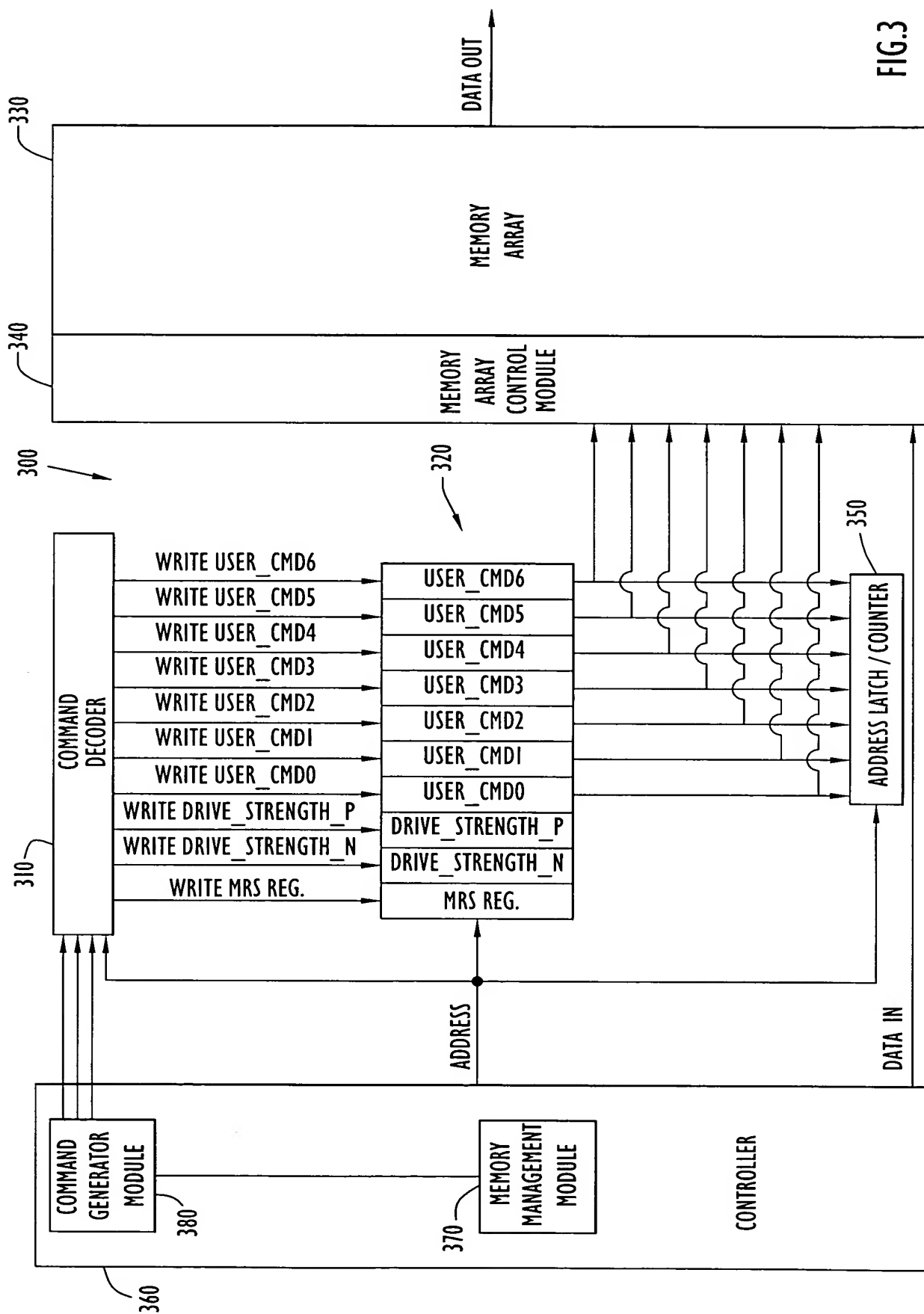


FIG.2



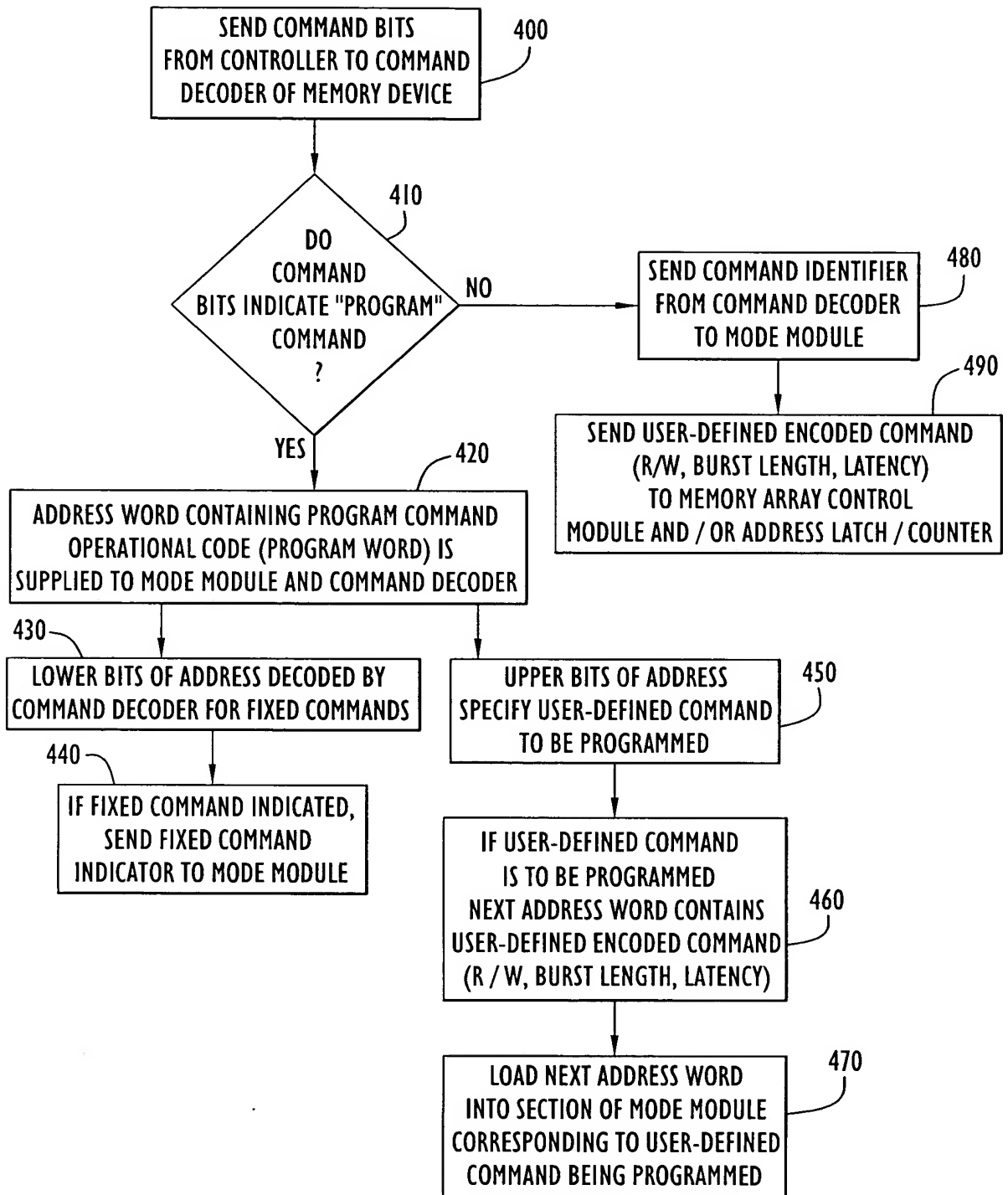


FIG.4

CMD[2:0]	COMMAND	ADDRESS
0	FIXED_COMMAND/PROGRAM	OP_CODE
1	USER_CMD0	A
2	USER_CMD1	A
3	USER_CMD2	A
4	USER_CMD3	A
5	USER_CMD4	A
6	USER_CMD5	A
7	USER_CMD6	A

FIG.5

ADDRESS	COMMAND	DESCRIPTION
0	NOP	CHIP DESELECT / NO OPERATION
1	AUTO REFRESH	AUTO REFRESH COMMAND
2	MRS	MODE REGISTER SET
3	N_DRIVE	DRIVE_STRENGTH_N
4	P_DRIVE	DRIVE_STRENGTH_P
5-15	RESERVED	X
16	USER_CMD0	COMMAND_DEFINITION
17	USER_CMD1	COMMAND_DEFINITION
18	USER_CMD2	COMMAND_DEFINITION
19	USER_CMD3	COMMAND_DEFINITION
20	USER_CMD4	COMMAND_DEFINITION
21	USER_CMD5	COMMAND_DEFINITION
22	USER_CMD6	COMMAND_DEFINITION
23-MAX	RESERVED	X

FIG.6

BITS	DESCRIPTION
0	0 = DLL DISABLED 1 = DLL ENABLED
1	0 = ADDRESS NON-MULTIPLEXED 1 = ADDRESS MULTIPLEXED
2	0 = 50 OHM INTERNAL CALIBRATION 1 = EXTERNAL CALIBRATION RESISTOR
3	0 = ON DIE TERMINATION DISABLED 1 = ON DIE TERMINATION ENABLED
4-MAX	RESERVED

**FIG.7**

BITS:	DESCRIPTION:
3:0	READ LATENCY
7:4	WRITE LATENCY
11:8	BURST LATENCY
15:12	COMMAND
20:16	RESERVED

**FIG.8**

ENCODING	READ / WRITE LATENCY
0-1	RESERVED
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9-15	RESERVED

**FIG.9**

ENCODING	BURST LENGTH
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7-14	RESERVED
15	FULL PAGE

**FIG.10**

ENCODING	COMMAND
0	TERMINATE
1	READ
2-8	RESERVED
9	WRITE
10-15	RESERVED

**FIG.11**